

0976390-000000

The diagram illustrates a multi-stage MOSFET amplifier circuit, labeled 10. It consists of three main stages: a first stage (22), a second stage (24), and a third stage (28).

- First Stage (22):** This stage uses two NMOS transistors,  $Q_1$  and  $Q_2$ . The gates of  $Q_1$  and  $Q_2$  are connected to a common input node. The source of  $Q_1$  is connected to ground, and the source of  $Q_2$  is connected to the source of  $Q_1$ . The gates of  $Q_1$  and  $Q_2$  are biased by  $V_{CC1}$ . The input voltages  $v_{1+}$  and  $v_{1-}$  are applied to the gates of  $Q_1$  and  $Q_2$  respectively.
- Second Stage (24):** This stage uses two NMOS transistors,  $Q_3$  and  $Q_4$ . The gates of  $Q_3$  and  $Q_4$  are connected to a common input node. The source of  $Q_3$  is connected to ground, and the source of  $Q_4$  is connected to the source of  $Q_3$ . The gates of  $Q_3$  and  $Q_4$  are biased by  $V_{CC2}$ . The input voltages  $v_{2+}$  and  $v_{2-}$  are applied to the gates of  $Q_3$  and  $Q_4$  respectively.
- Third Stage (28):** This stage uses two NMOS transistors,  $Q_5$  and  $Q_6$ . The gates of  $Q_5$  and  $Q_6$  are connected to a common input node. The source of  $Q_5$  is connected to ground, and the source of  $Q_6$  is connected to the source of  $Q_5$ . The gates of  $Q_5$  and  $Q_6$  are biased by  $V_{BIAS1}$  and  $V_{BIAS2}$  respectively.

A common source resistor is connected to ground. The circuit is labeled with various components and reference numerals:  $V_{CC1}$ ,  $V_{CC2}$ ,  $V_{BIAS1}$ ,  $V_{BIAS2}$ ,  $Q_1$ ,  $Q_2$ ,  $Q_3$ ,  $Q_4$ ,  $Q_5$ ,  $Q_6$ ,  $v_{1+}$ ,  $v_{1-}$ ,  $v_{2+}$ ,  $v_{2-}$ , and  $v_{1-}$ .

Figueres

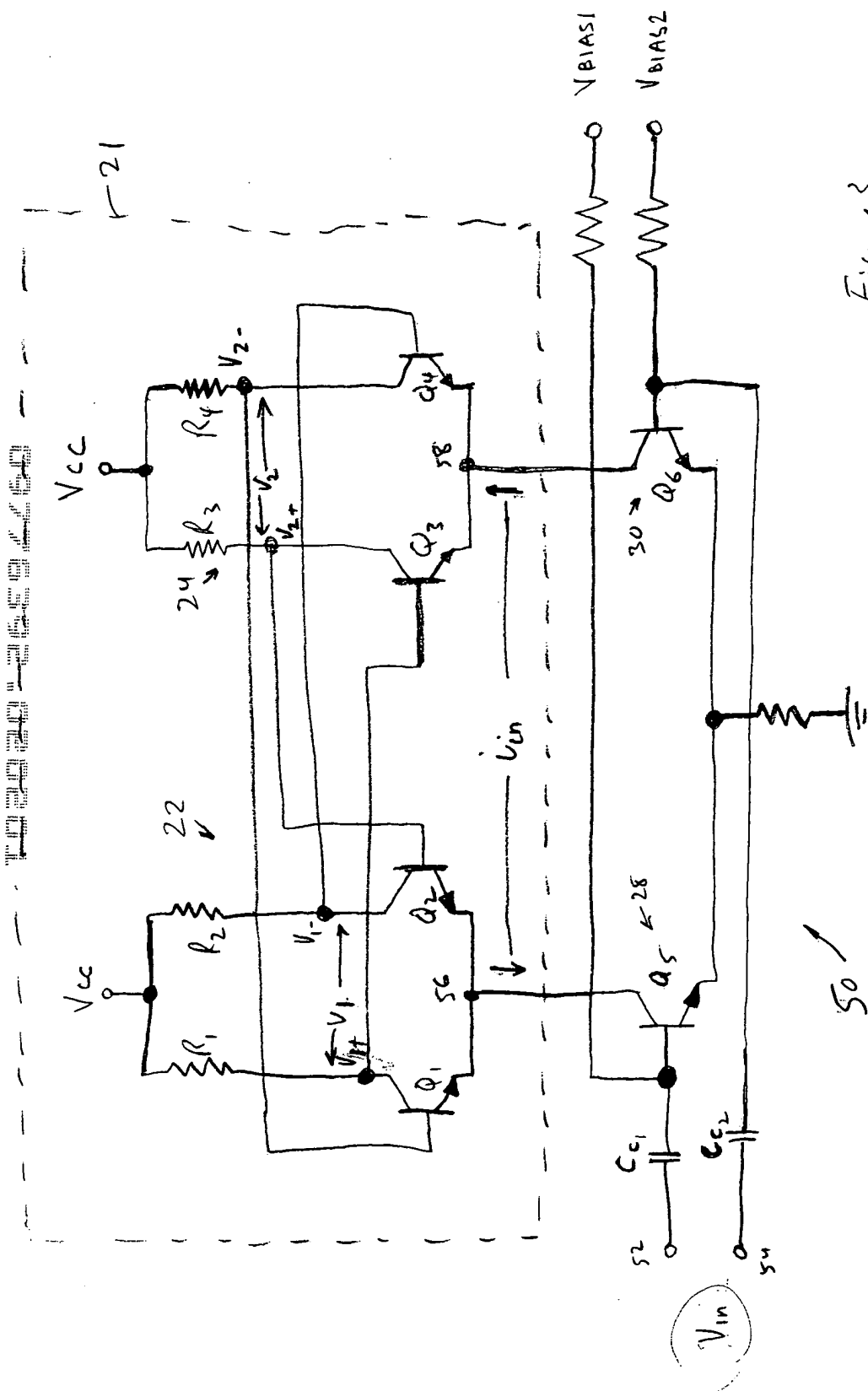


Figure 3

RF<sub>in</sub>

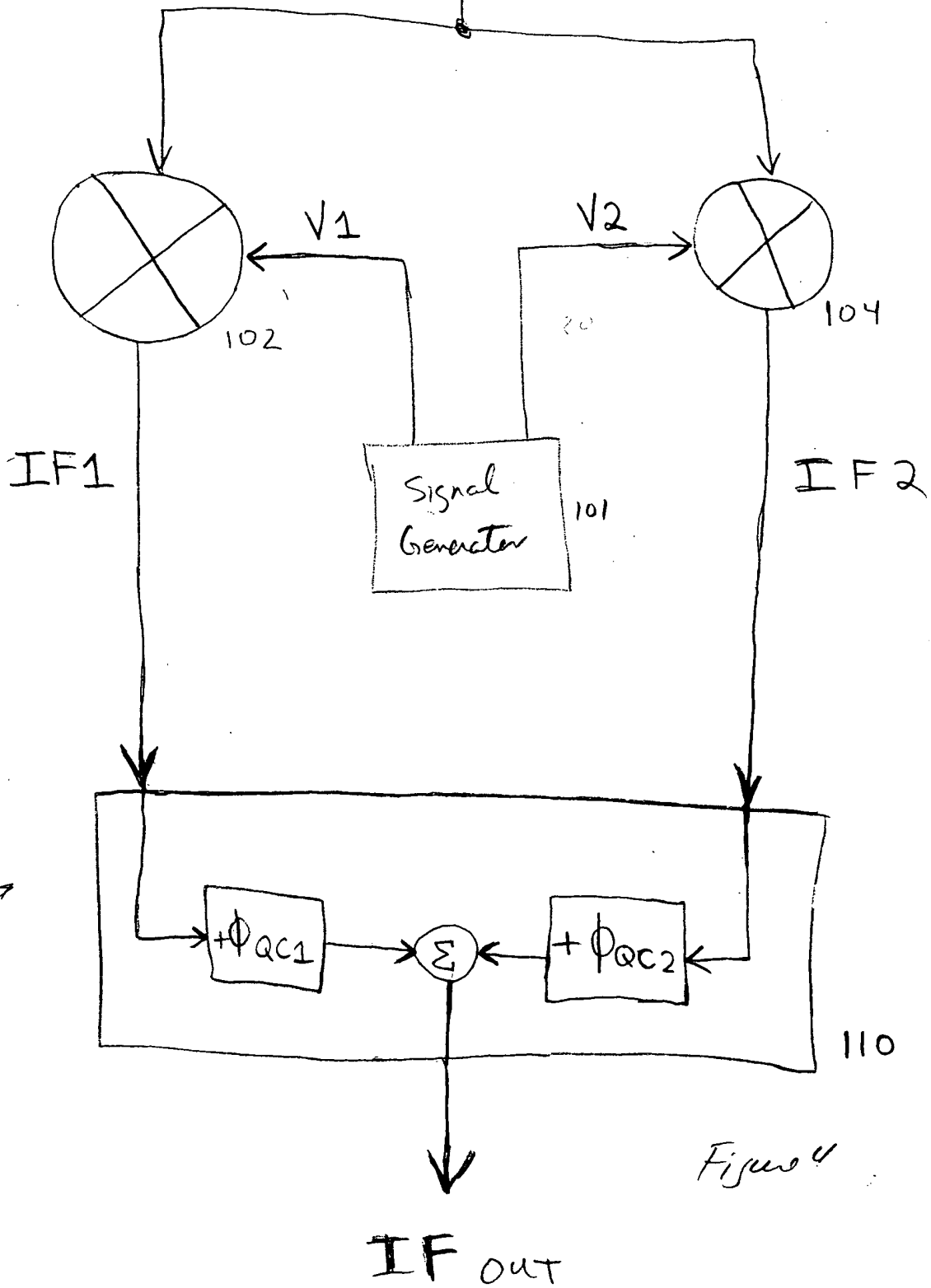


Figure 4

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